

FIG. 1 RELATED ART

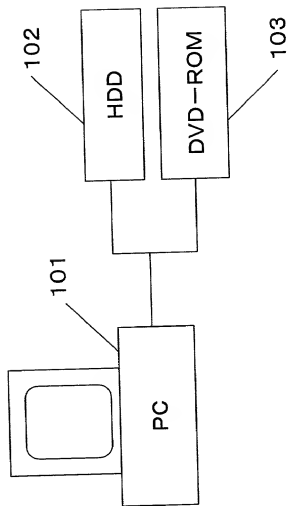


FIG. 2 RELATED ART

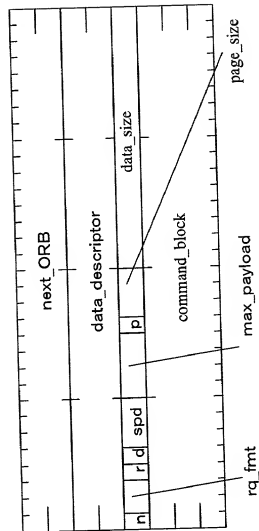
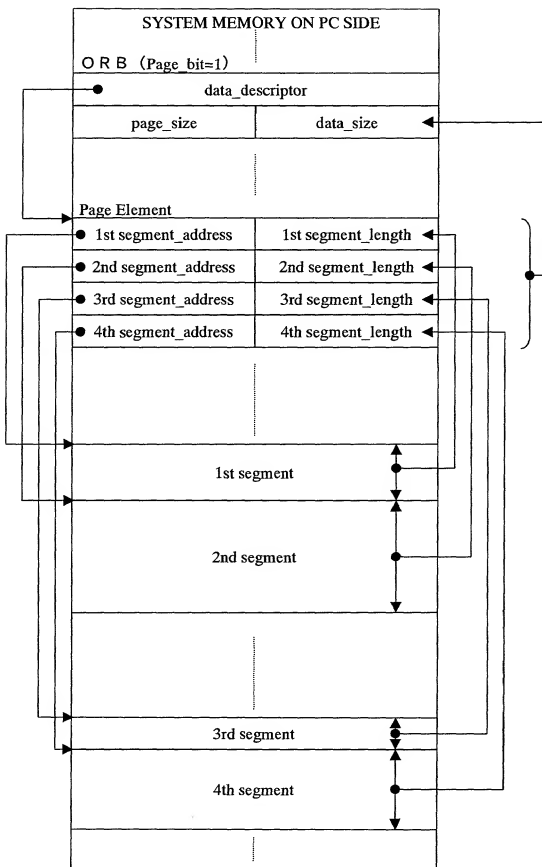




FIG. 4 RELATED ART



0000302.1.2.01

FIG. 5 RELATED ART

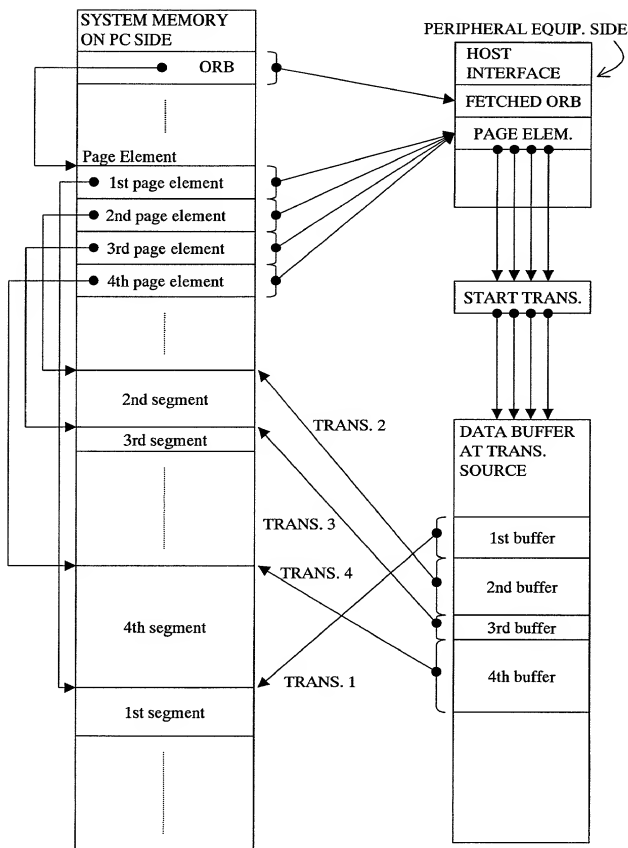


FIG. 6

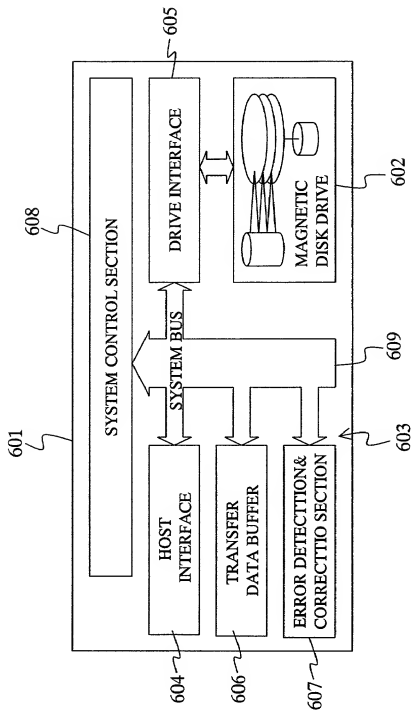


FIG. 7

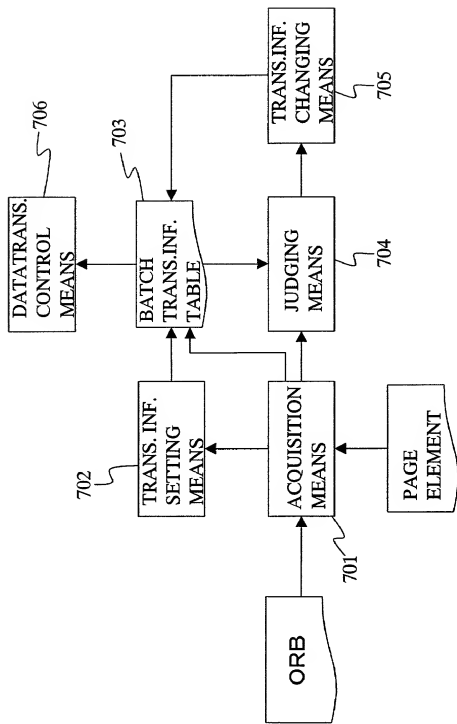


FIG. 8

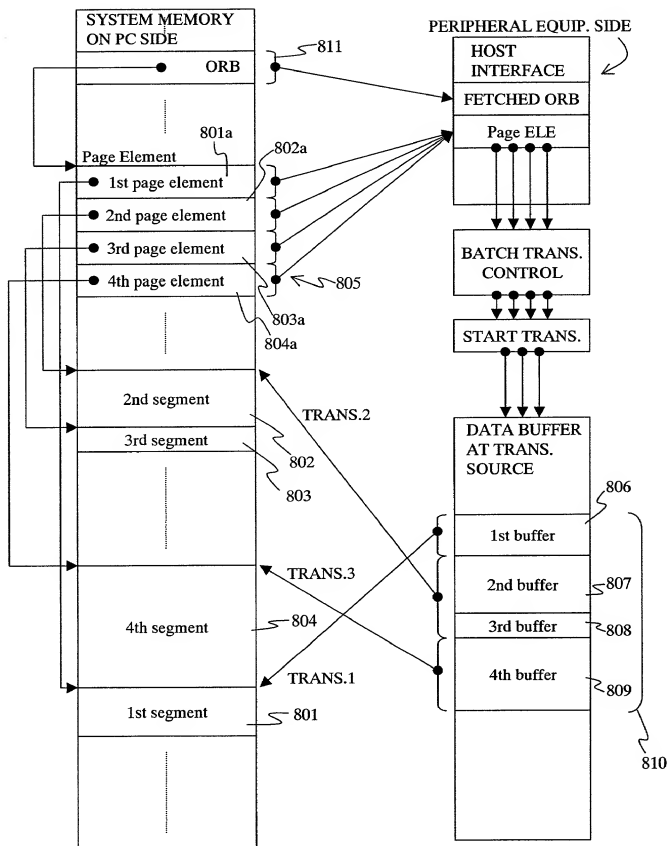




FIG. 9A

703

page_counter	segment_base_hi
segment_base_lo	
buffer_point	
transfer_length	

FIG. 9B

703

page_counter = data_size	1st segment_base_hi
1st segment_base_lo	
buffer_point=Logical Block Address	
transfer_length = 1st segment_length	

FIG. 10A

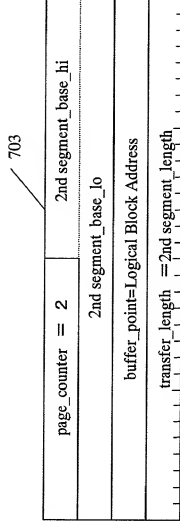


FIG. 10B

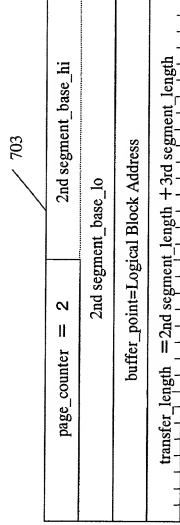
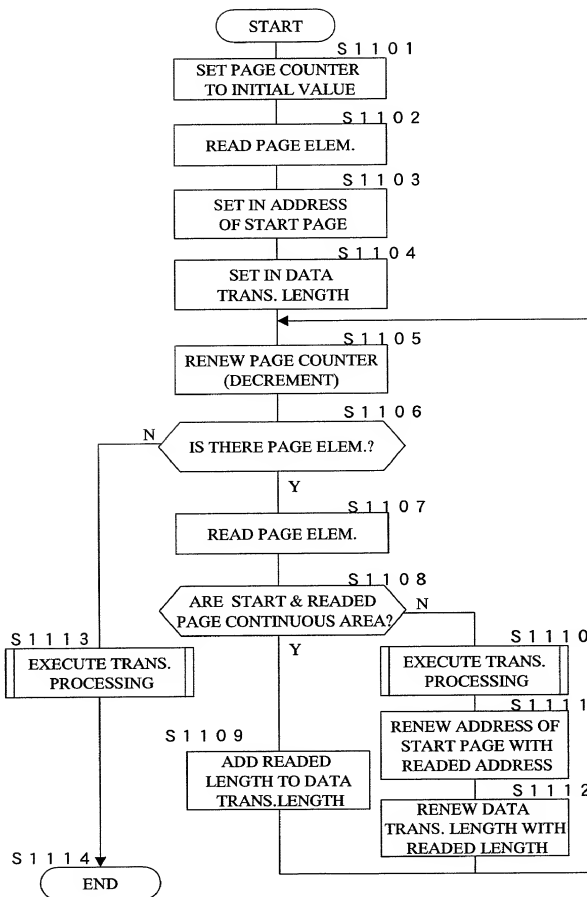
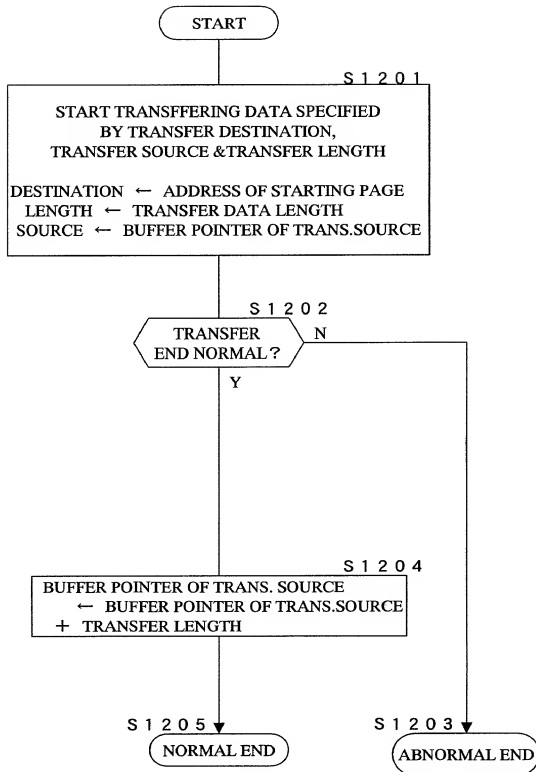


FIG. 11



101217-20255550

FIG. 12



00000000 112101

FIG. 13

703

start_page	end_page	transfer_length	page_counter
buffer_point			
1st segment_length		1st segment_base_lo	1st segment_base_hi
1st segment_base_lo			
2nd segment_length		2nd segment_base_lo	2nd segment_base_hi
2nd segment_base_lo			
.....			
nth segment_length		nth segment_base_lo	nth segment_base_hi
nth segment_base_lo			

FIG. 14

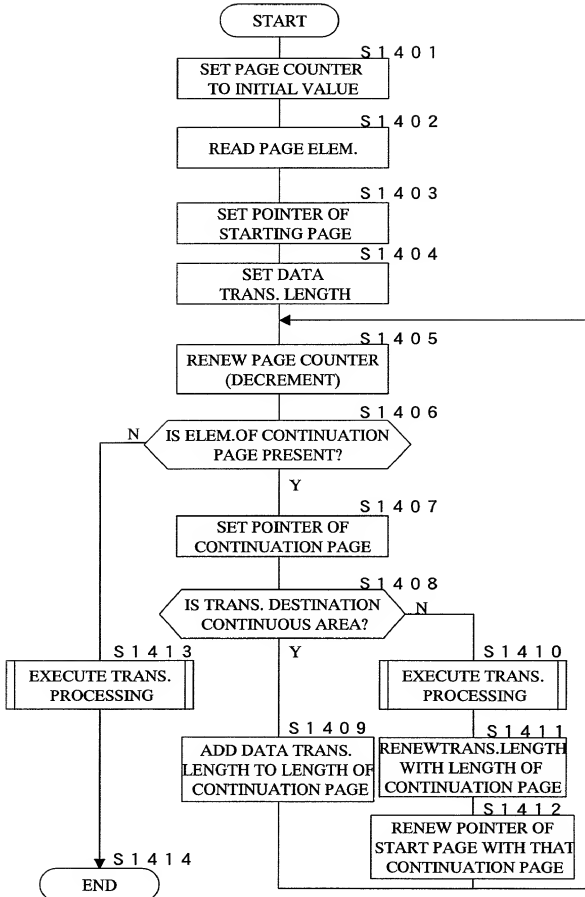


FIG. 15

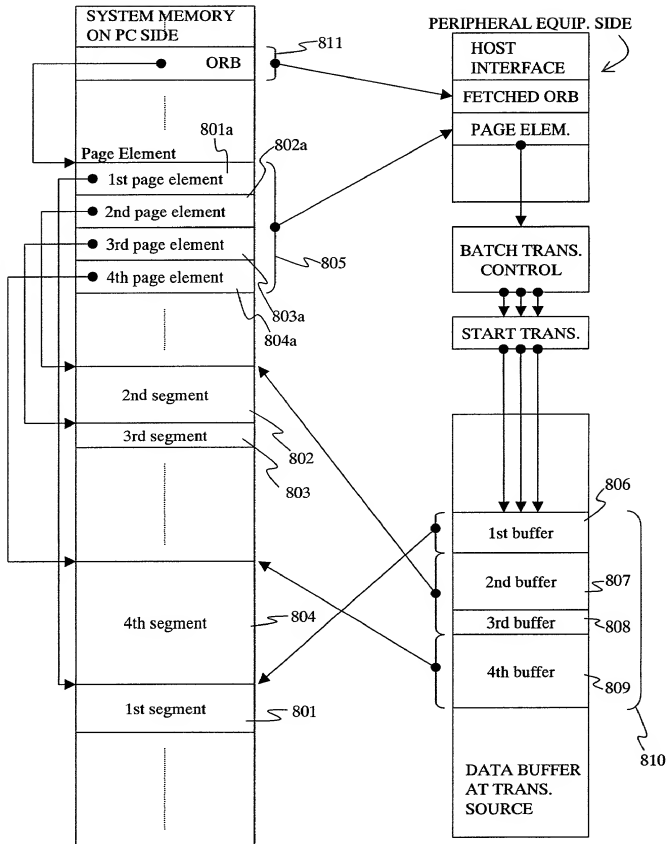


FIG. 16

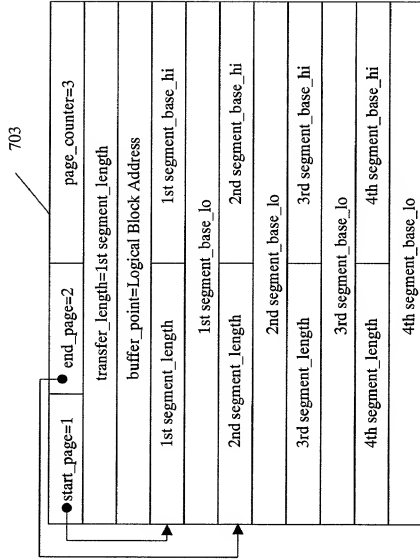




FIG. 17

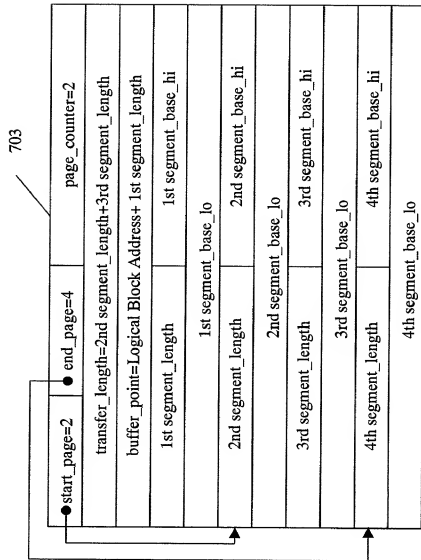


FIG. 18

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start_page	end_page	page_counter
transfer_length		
1st segment_length		1st segment_base_hi
1st segment_base_lo		
1st buffer_point		
2nd segment_length		2nd segment_base_hi
2nd segment_base_lo		
2nd buffer_point		
.....		
nth segment_length		nth segment_base_hi
nth segment_base_lo		
nth buffer_point		

FIG. 19

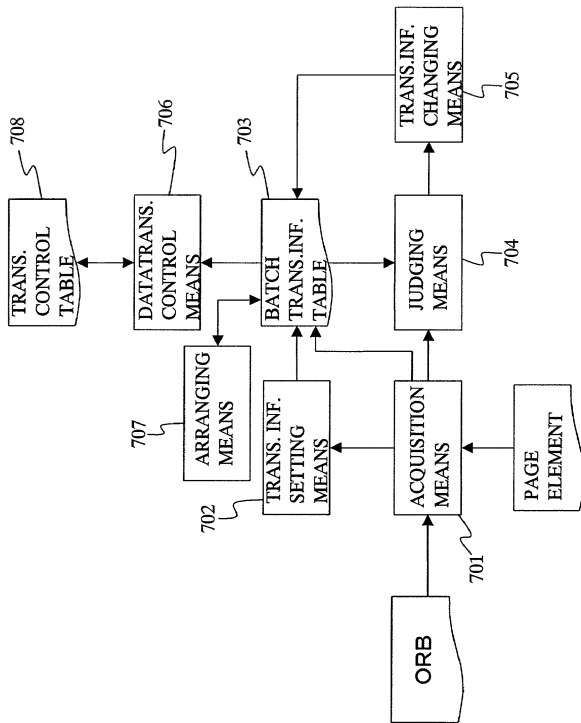


FIG. 20

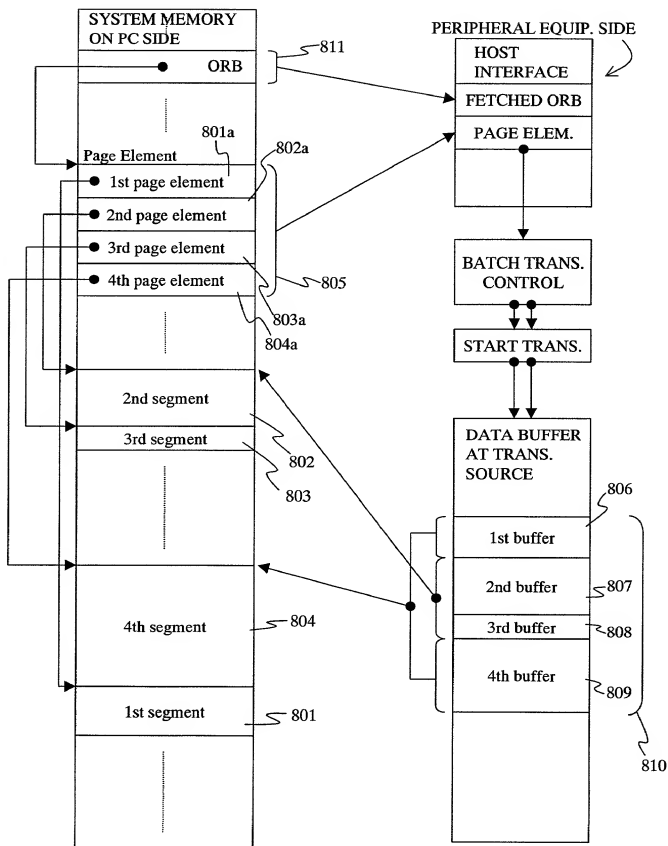


FIG. 21

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●start_page=1	end_page=0	page_counter=4
transfer_length=2nd segment_length		
2nd segment_length	2nd segment_base_hi	
2nd segment_base_lo		
2nd buffer_point		
3rd segment_length	3rd segment_base_hi	
3rd segment_base_lo		
3rd buffer_point		
4th segment_length	4th segment_base_hi	
4th segment_base_lo		
4th buffer_point		
1st segment_length	1st segment_base_hi	
1st segment_base_lo		
1st buffer_point		

FIG. 22

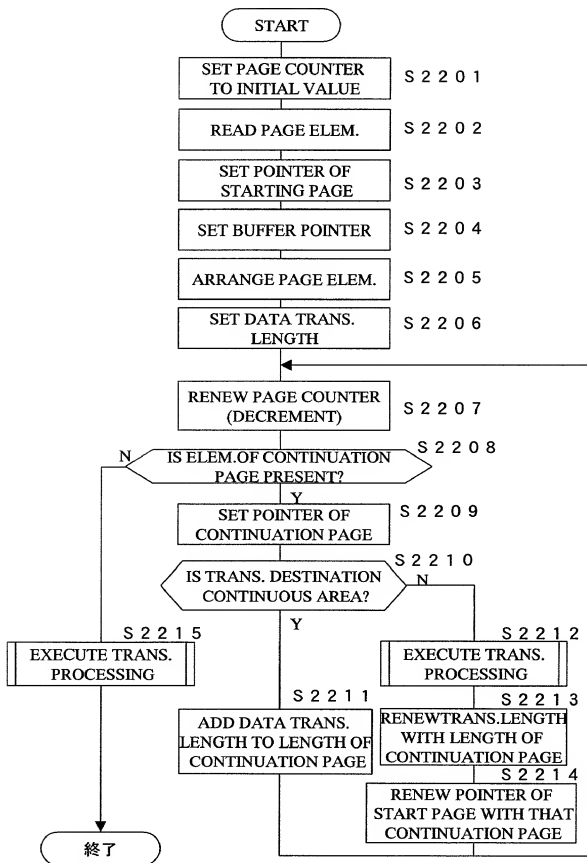


FIG. 23

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● start_page=1	end_page=0	page_counter=4
transfer_length=0		
1st segment_length	1st segment_base_hi	
1st segment_base_lo		
1st buffer_point=Logical Block Address		
2nd segment_length	2nd segment_base_hi	
2nd segment_base_lo		
2nd buffer_point= 1st buffer_point+2nd segment_length		
3rd segment_length	3rd segment_base_hi	
3rd segment_base_lo		
3rd buffer_point= 2nd buffer_point+3rd segment_length		
4th segment_length	4th segment_base_hi	
4th segment_base_lo		
4th buffer_point= 3rd buffer_point+4th segment_length		

FIG. 24

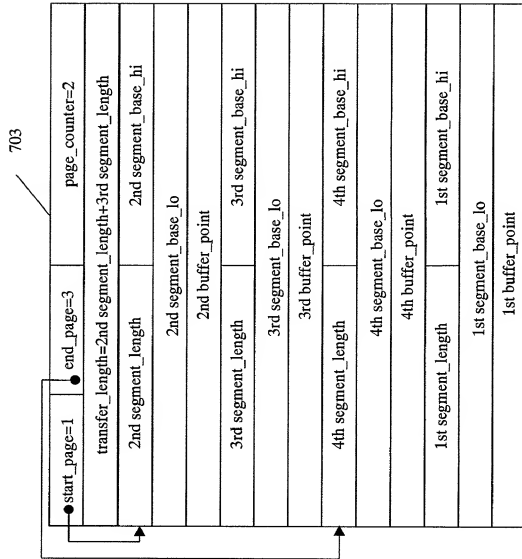




FIG. 25

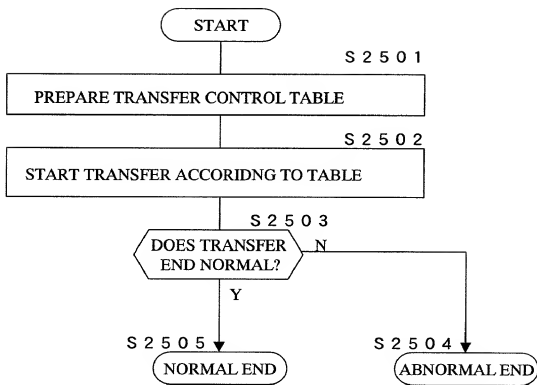


FIG. 26

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buffer_number	start segment_base_hi
start segment_base_lo	
buffer_length 1	buffer_length 2
.....	.....
buffer_length n-1	buffer_length n
buffer_address 1	
buffer_address 2	
.....	
buffer_address n	
.....	

FIG. 27

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buffer_number = 2	2nd segment_base_hi
2nd segment_base_lo	
buffer_length_1=2nd segment_length	buffer_length_2=3rd segment_length
buffer_address_1 = 2nd buffer_point	
buffer_address_2 = 3rd buffer_point	

FIG. 28

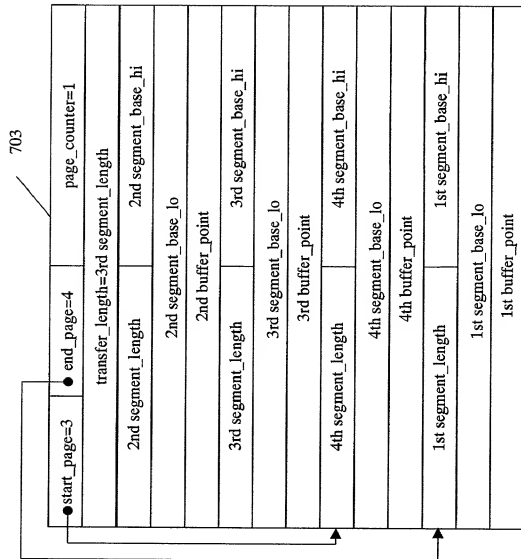


FIG. 29

Host	1st	2nd	3rd	Last1	Last
CD9050		1	1	1	1
186D000	14	15	15	15	15
186D000	13	14	14	14	14
186D000	15	16	16	16	16
1870000	12	13	13	13	13
1871000					
1872000					
1873000	11	12	12	12	12
1874000					
1875000	10	11	11	11	11
1876000	9	10	10	10	10
1877000					
1878000					
1879000					
187A000					
187B000	6	7	7	7	7
187C000					
187D000					
187E000	5	6	6	6	6
187F000	7	8	8	8	8
1880000	4	5	5	5	5
1881000	8	9	9	9	9
1882000	3	4	4	4	4
1883000					
1884000	2	3	3	3	3
1885000					
1886000		2	2	2	2
1886500	1				
1893000	16				

101211.2036666



[illegible]